An Accurate Equivalent Circuit Model of Flip Chip Interconnects

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ABSTRACT

In this paper, a general and accurate circuit model of the flip chip interconnect has been investigated and presented. In this circuit model, statistical analysis is used to compute the value of the circuit elements. Also, losses in the flip chip package are represented by a simple function vs frequency. These losses include substrate loss of the chip and the mother board due to excitation of surface wave and radiation loss due to the bump. Good agreement has been obtained between the s-parameters of the FD-TD model and the equivalent circuit model over a wide frequency band of up to 50 GHz. This equivalent circuit can be used in commercial circuit simulators to predict MMIC performance including the package.

I. Introduction

Flip chip is emerging as the lead technology in multi-chip module packages. Several chips can be mounted together to the mother board using flip chip technology to increase density, improve system performance and reduce cost [1]. This packaging technique also allows combinations of active and passive devices, silicon and gallium arsenide, and probably analog and digital circuits in the same application. In microwave circuits applications, low cost, high density and short transition interconnects are considered to be the main advantages of the flip chip technique. Transitions in a flip chip package involve the use of metallic bumps (or via holes) to transmit the signal between the mother board and the chip. These bumps represent the main discontinuity to the signal propagating on the line which results in partial loss, reflection and possibly distortion of the signal. All these issues need to be considered in the design of the flip chip package.

This work is mainly concerned with the analysis and characterization of the flip chip package discontinuities using FD-TD method with the objective of developing an equivalent circuit model of the bump discontinuities over a broad frequency band. An equivalent circuit model of the flip chip discontinuity will be a helpful tool in using commercial MMIC simulators to predict the overall performance including the package. In the literature, few papers have been published on the equivalent circuit model of the bump discontinuities [2-3]. However, the effects of the flip-chip technique are not clear. In this paper, we investigated and modeled the effects of the bump transition on the package performance In our analysis, a flip chip CPW package configuration is considered. In this configuration, the transition between two CPW lines on the chip and the mother board is investigated, and it is referred to as CPW-CPW transition as shown in fig.1. Section II of this paper presents a brief discussion of FD-TD method used for analysis and modeling. This includes the excitation source requirements and boundary condition treatment. The S-parameters are also discussed in this section. In section III, statistical analysis is used to develop an equivalent circuit model of flip chip interconnects. Results of s-parameters of the flip chip transitions as compared to the equivalent circuit model are presented in section IV, and section-V concluded the present paper.

II. Finite-Difference Time-Domain Method

An alternating technique to the frequency-domain analysis and modeling of several engineering problems is the Finite-Difference Time-Domain (FD-TD) method. This method is well known in principle since 1966 [4]. In microwave circuit applications, FD-TD technique has been widely used in the analysis of microwave devices. Recently, FD-TD method has been effectively used to model the transition effects of high frequency interconnect in a flip chip package [5-6]. FD-TD method is attractive due to its flexibility in handling a variety of

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circuits configurations. An additional benefit of the time-domain analysis is that a broad band pulse can be used as the excitation, and the frequency-domain response can be evaluated over a broad of frequencies by means of Fourier discrete transform of the transient response. In our analysis, we assume that media under consideration are uniform, isotropic, homogeneous and has no magnetic properties, i.e., $\mu_r \equiv 1$. Furthermore, we assume that ground and center conductors are perfect conductors (PEC) and have zero thickness. A gaussian pulse is used to modulate the transverse spatial distribution of the excitation fields as

$$E_x(x,y)=\psi_x(x,y).\exp\left(-(t-t_o)^2/T^2\right) \quad (1)$$

$$E_y(x,y)=\psi_y(x,y).\exp\left(-(t-t_o)^2/T^2\right) \quad (2)$$

Where,

$\psi_x(x,y)$ The spatial distribution function for x-component of the electric field.

$\psi_y(x,y)$ The spatial distribution function for y-component of the electric field.

t_o Time center of the pulse.

T Pulse width.

The spatial distribution functions, $\psi_x(x,y)$ and $\psi_y(x,y)$, are not initially known. However, a quasi-static TEM mode assumption can be used as initial guess. In this work, a quasi-static distribution is launched in a CPW structure with the same dielectric layers as the flip chip structure. The length of this CPW will be assumed as the reference in our calculations and is chosen such that the mode will be developed at the output. This output is then used as the correct spatial distribution functions $\psi_x(x,y)$ and $\psi_y(x,y)$ for all flip chip structures in our simulation.

To simulate infinite structures, absorbing boundary conditions (ABC's) have to be added at the six outer walls of the computational domain. There are different techniques for simulating an ABC. In our simulation, we used the super-absorption first-order Mur boundary conditions due to its simplicity and stability [7]. At the source plane, we apply the excitation field components (E_x and E_y)until the pulse is completely lunched, and then, switch to the ABC to avoid reflection from the source plane. Another boundary treatment is the air-dielectric interface where, the average dielectric constant is used, i.e., $(\varepsilon_1+\varepsilon_2)/2$. Furthermore, in our simulation a technique of non-uniform mesh is used to reduce the memory requirement as well as to reduce the CPU time.

The effects of the flip-chip interconnects can be characterized by evaluating the S-parameters. A new definition of the s-parameters based on power calculation is defined as

$$Sij(w)=\sqrt{\frac{V_i^-(z_i,w)I_i^-(z_i,w)}{V_j^+(z_j,w)I_j^+(z_j,w)}} \quad (3)$$

Where,

V_i^- denotes the reflected voltage at the port (i).

V_j^+ denotes the incident voltage at the port (j).

I_i^- denotes the reflected current at the port.(i).

I_j^+ denotes the incident current at the port.(j).

The above definition of s-parameters have been useful in reducing the numerical errors due to ABC to a second order effect.

III. Equivalent Circuit Model

A general circuit model of a single transition interconnect is shown in fig.(2). This model represents the transition interconnects between the chip and the mother board including losses. These losses include substrate loss and radiation loss. In general, substrate loss is due to the excitation of surface waves in the dielectric material, and it can be significant at high frequencies. The interconnect loss is due to radiation of the bump and the open end of the CPW lines. Conductor loss can be also included in the model. These losses are usually a function vs. frequency. The Y-parameters of the equivalent circuit model is given by

$$Y_{11}(w)=y_b(w)+y_1(w) \quad (4\text{-a})$$

$$Y_{22}(w)=y_b(w)+y_2(w) \quad (4\text{-b})$$

$$Y_{12}(w)=-y_b(w) \quad (4\text{-c})$$

$$Y_{21}(w)=-y_b(w) \quad (4\text{-d})$$

where,

$$Y_1(w)=G_1(w)+jwC_1 \quad (5\text{-a})$$

$$Y_2(w)=G_2(w)+jwC_2 \quad (5\text{-b})$$

$$Y_b(w)=G_b(w)+1/jwL_b \quad (5\text{-c})$$

where,

L_b denotes the inductance of the bump.

G_b denotes the radiation conductance.

C_1 denotes the discontinuity capacitance at the mother board.

C_2 denotes the discontinuity capacitance at the chip.

G_1 denotes substrate loss conductance of the mother board.

G_2 denotes substrate loss conductance of the chip.

To find the value of the above elements, a matching algorithm is used. In this algorithm the scattering parameters of

the interconnects obtained from the FD-TD are converted to the Y-parameters. The Y-parameters is then used to find the elements of the PI equivalent circuit using equations 4 and 5. Statistical analysis is used to find an average or the rms value whenever this is possible, or a simple function to approximately represent the frequency dependence. The following is the algorithm used to match the s-parameters of the circuit model:

(1) Compute the mean value of the characteristic impedance of the reference transmission line over the entire frequency band.

(2) Compute the mean values of the capacitance and the inductance over the entire frequency band.

(3) Radiation conductance is represented by $G_b(w)=K_b/f^2$, where K_b is constant computed as the mean value over the entire frequency band.

(4) Substrate loss conductance is approximated as

$$G_{1,2}(w)=K_{go1,2} \qquad f \le f_{o1,2}$$

$$= K_{go1,2} + K_{g1,2}(f - f_{o1,2})^2 \qquad f \ge f_{o1,2}$$

where,

$G_{1,2}(.)$ are the substrate losses of the chip and mother board.

$K_{go1,2}$ and $K_{g1,2}$ are constants computed for a broad band frequency response.

$f_{o1,2}$ are the corner frequencies at which substrate losses of chip and mother board start to creep up.

Finally, the s-parameters of the circuit model are calculated and compared to the FD-TD parameters.

IV. Results

The s-parameters of a CPW to CPW transition has been investigated using FD-TD as discussed in Sec. II. The geometry and dimensions of the transition are shown in Fig. 1. An equivalent circuit model of the transition has been developed as discussed in Sec. III. Table(1) includes the values of the lumped elements in the circuit model. Then, the s-parameters based on the equivalent circuit is evaluated using a circuit solver and compared to the FD-TD results. The s-parameters of the circuit model and the FD-TD model of the flip chip package are presented in fig.3. As evident from the figure, a good agreement has been obtained up to 50 GHz between the s-parameters of both models. The difference in the computed S_{11} between the statistical and FDTD model is less than 3% (less 1.0 dB) over a wide frequency band (up to 50 GHz). The difference in S_{12} is less than 2% (less 0.05 dB) up to 50 GHz.

V. Conclusion

A Three dimensional finite difference time domain computer code has been developed to model and investigate the transition discontinuities in the flip chip package. The s-parameters based on the FD-TD model is used to develop an equivalent circuit for the interconnect. Using a circuit solver, the s-parameters of the equivalent circuit are compared and verified vs the FD-TD predictions over a broad band of frequencies.

References

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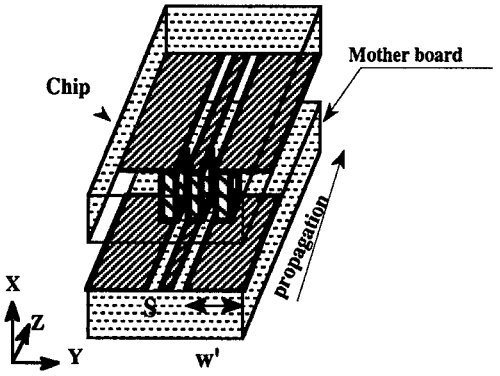
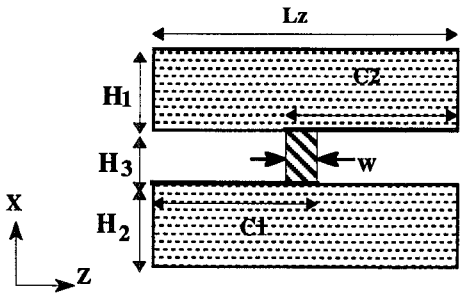
Table(1) Elements values of the equivalent circuit model

L_b	0.020734 nH
$C_1 = C_2$	0.0231301 pf



(a) Three dimensional view



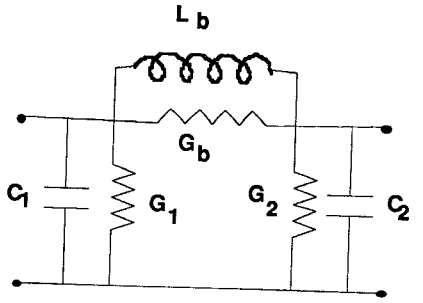
(b) Side view

Figure(1) Geometry of flip chip CPW-CPW transition

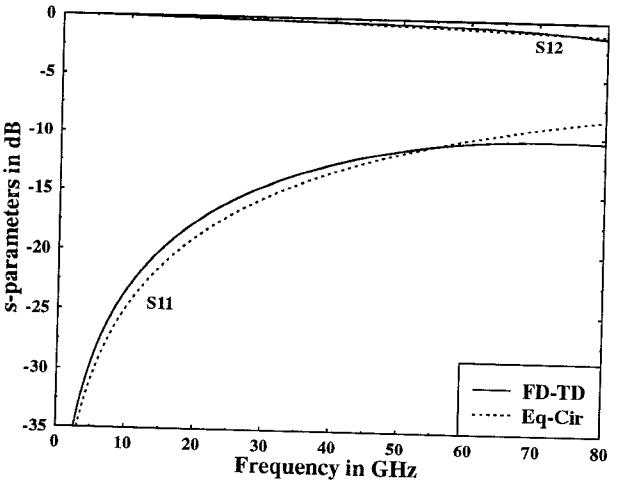
$H_1 = H_2 = 0.36mm$, $H_3 = S = W = 0.12mm$

$C_1 = 3.12mm$, $C_2 = 2.16mm$, $L_z = 5.04mm$

$W' = 0.6mm$



Figure(2) Equivalent Circuit model



Figure(3) S-parameters of flip chip CPW-CPW transition and the equivalent circuit